ABSTRACT OF THE DISCLOSURE

The present invention is related to a method for estimating power consumption and noise levels of an integrated circuit which is composed of logic gates connected in the form of a plurality of stages. (1) At the outset, output signal waveforms and occurrence probabilities thereof at the first stage of the logic gates are calculated by the use of signal waveforms and occurrence probabilities thereof at primary input terminals of the integrated circuit; (2) next, output signal waveforms and occurrence probabilities thereof at the second stage of the logic gates are calculated by the use of the output signal waveform and the occurrence probability thereof at the primary input terminals and the output signal waveform and the occurrence probability thereof at the first stage of the logic gates; and (3) then, output signal waveforms and occurrence probabilities thereof at the n-th stage (n is a natural number) of the logic gates are calculated by the use of the output signal waveform and the occurrence probability thereof at the primary input terminals and the output signal waveform and the occurrence probability thereof at the (n-1)th stage of the logic gates. Thereby, types of the respective elementary waveforms, occurrence probabilities and signal correlations are calculated relating to signals located on each wiring of each stage inside of the integrated circuit and occurring within a predetermined time period.